AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A cache comprising:

a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays and a redundant array;

a bus having data lines to transmit information from the regular arrays and to transmit information from the redundant array; and

circuitry to connect a first set of information from the regular array to a first set of the data lines and to connect a second set of information from the regular array and the redundant array to a second set of the data lines.

2. (Original) The cache of claim 1 wherein the circuitry comprises a bit that, when set to a first logic state, causes the circuitry to disconnect the regular array from the bus.

3. (Original) The cache of claim 2 wherein the circuitry is further operative to connect the redundant array to the bus responsive to the bit being set.

4. (Original) The cache of claim 1 wherein the arrays in a bank are arranged linearly.

5. (Original) The cache of claim 1 wherein the arrays in a bank are arranged in multiple rows.

6. (Original) The cache of claim 2, further comprising:

a plurality of repeaters each of which provides for series connection of an array with a data line of the bus.

7. (Previously Presented) A cache, comprising:

a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays, A_{0-N}, and a redundant array;

a data bus having N+1 sets of bus lines, B_{0-N}, to communicate data from the regular arrays and to said redundant array;

logic associated with each array to communicate data from an i^{th} regular array to an i^{th} set of the bus lines, with the redundant array being disconnected from the data bus, wherein the logic is to disconnect the regular array, A_i, from the data bus and to connect the redundant array to the data bus in response to a change in state of a bit associated with a cache bank.

8. (Original) The cache of claim 7 wherein the arrays in a bank are arranged linearly, regular arrays, A_0 to $A_{(i-1)}$ connect to bus lines B_0 to $B_{(i-1)}$, respectively, and regular arrays, $A_{(i+1)}$ to A_N connect to bus lines B_i to $B_{(N-1)}$, respectively, responsive to the change.

9. (Original) The cache of claim 7 wherein the arrays in a bank are arranged in multiple rows.

10. (Previously Presented) The cache of claim 7 wherein the logic includes a fuse circuit having a fuse, when the fuse is in a first conductivity state, the bit setting corresponding to the first state, and when the fuse is in a second conductivity state, the bit setting corresponding to the changed state.

11. (Original) The cache of claim 10, further comprising a plurality of repeaters each of which provides for series connection of an array with a data line of the bus.

12. (Previously Presented) A method comprising:

changing a bit associated with a cache bank from a first to a second logic state, the cache bank comprising a plurality of arrays of memory cells, the arrays including regular arrays, A_{0-N}, and a redundant array, data from the regular arrays being transmitted on corresponding bus lines, B_{0-N}, of a data bus when the bit is in the first logic state;

discontinuing transmitting data from a regular array, A_i, on the data bus in response to the single bit state being changed to the second logic state; and

transmitting data from the redundant array on the data bus in response to the bit state being changed to the second logic state.

13. (Original) The method of claim 12 wherein the data bus is unaffected by the single bit state being changed to the second logic state.

14. (Original) The method of claim 12 wherein changing the single bit state comprises blowing a fuse.

15. (Original) The method of claim 12 wherein the cache bank further comprises a plurality of repeaters each of which provides for series connection of an array with a data line of the data bus.